REMARKS

Reconsideration and allowance of the above-identified application are respectfully requested.

Claims 88-135 are currently pending, wherein claims 88, 97, 106, 115, 122 and 129 are independent. Claims 91, 100, 109, 118, 125, 132 and 136-198 have been canceled. Applicants reserve the right to file divisional applications to the non-elected inventions. Claims 88, 97, 106, 115, 122 and 129 have been amended to incorporate the features of claims 91, 100, 109, 118, 125, 132, respectively.

Claims 92, 101, 110, 119, 126 and 133 have been amended merely to change the dependency of these claims. These amendments do not narrow or otherwise limit the scope of these claims, are not made for any purpose related to patentability, and are fully supported by the present application. No new matter has been introduced by way of any of the amendments.

Applicants note with appreciation the acknowledgement by the Patent Office of the Information Disclosure Statement filed on December 12, 2003.

In the second section of the Office Action, claims 88-90, 92-99, 101-108, 110-117, 119-124, 126-131 and 133-135 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Shinichi (U.S. Patent No. 4,959,698, hereinafter "Shinichi"). This rejection is respectfully traversed.

Exemplary embodiments of the present invention are directed to an apparatus and method for improving signal-to-noise ratio and reducing overall bit line capacitance and area in a dynamic random access memory (DRAM). Because the manufacturing process for

DRAM cells involves a deep submicron geometry, gate leakage and tunneling leakage are high. Therefore, it is desirable not to needlessly waste any area of the DRAM cell. By minimizing the wasted area, the leakage problems are also minimized. As illustrated in Figure 10 of the present application, the transistor gate 905 is connected to the substrate 910 by a gate oxide 915, and the substrate 910 includes a diffusion layer 930. However, the cell plate 920 is physically located at a horizontally overlapping position relative to the gate 905, so that there is no lateral spacing between the cell plate 920 and the gate 905. For example, the cell plate 920 can be located at a vertical offset from the gate 905. The cell plate 920 and the gate 905 can be viewed as being on separate vertical levels, as seen from the substrate 910. This vertical offset causes a decreased capacitance between the cell plate 920 and the substrate 910, and, in this context, it is preferable not to decrease the capacitance. *To reduce the adverse effect of the decreased capacitance caused by the vertical offset, a dielectric material 1005, preferably a material having a high dielectric constant, such as, for example, Si_3N_4, tantalum oxide, aluminum oxide or oxinitride, is used to fill in the space between the cell plate 920 and the substrate 910.* [*see* present application, page 17, paragraph 0038]

Figure 11 illustrates an alternative exemplary embodiment of a DRAM cell arrangement having reduced lateral spacing according to the present invention. As shown therein, a portion of the cell plate 920 overlaps the gate 905. A thin, high-dielectric-constant material 1005', such as, for example, Si_3N_4, tantalum oxide, aluminum oxide or oxinitride, is used to fill in the space between the cell plate 920 and the substrate 910. [*see* present application, page 18, paragraph 0039] Figure 12 illustrates another alternative exemplary embodiment of a DRAM cell arrangement having reduced lateral spacing according to the present invention. In this arrangement, a thin, high-dielectric-constant material 1005'', such

as, for example, Si_3N_4, tantalum oxide, aluminum oxide or oxinitride, is used to fill in the space between the cell plate 920 and the substrate 910. Cell plate 920 is separated laterally from gate 905 and diffusion layer 930' under that area. [*see* present application, page 18, paragraph 0040]

Shinichi discloses a memory cell of a semiconductor memory device. According to Shinichi, the memory cell includes one transistor and one capacitor. The transistor includes a first electrode formed as a diffused region at the center of the memory cell region and surrounded by an isolating region. The transistor also includes a gate electrode formed around the first electrode through a gate insulator on the major surface of the substrate. The capacitor region is formed between the gate electrode and the isolating region. A second electrode of the transistor can be formed of one of the electrodes of the capacitor. [*see* Shinichi, column 2, lines 14-26] As disclosed by Shinichi, the shape of the gate electrode prevents current leakage between the source and drain electrodes, as electron flow between the source and the drain is not parallel to the boundary of the isolating region. Another result of the structure is that change in threshold voltage of each transistor is prevented. [*see* Shinichi, column 2, lines 27-32]

According to Shinichi, a dielectric material (e.g., dielectric materials 105, 207, 307, 407, 507, 608, 708, 808) is used as an insulator. [*see, e.g.*, Shinichi, column 3, lines 28-30; column 3, lines 51-54; column 5, lines 13-15; and column 7, lines 30-32] However, in contrast to the present invention, it is respectfully submitted that *nowhere* does Shinichi disclose or suggest a dielectric material arranged between the cell plate, the gate and the substrate that comprises a high dielectric constant, as recited, for example, in claim 88 of the

present application. Therefore, it is respectfully submitted that Shinichi does not render the subject matter of claim 88 obvious.

The Patent Office asserts that "any dielectric material can be used in [the] Shinichi invention, e.g., SiO2 or silicon Nitride [sic] material, or a combination thereof, and that these material [sic] obviously including high dielectric constant inherently in them as well known in the art." [Office Action, page 3] According to M.P.E.P. § 2112, "[t]he fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic." [(citations omitted, emphasis in original)] More particularly,

> [t]o establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. [M.P.E.P. § 2112 (citations omitted)]

"In relying upon the theory of inherency, the examiner *must* provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." [M.P.E.P. § 2112 (emphasis added and in original)]

It is respectfully submitted that the Patent Office has provided *absolutely no* basis in fact and/or technical reasoning, *absolutely no* extrinsic evidence, and *absolutely no* support for its bald and unfounded assertion that Shinichi inherently discloses that the dielectric material comprises a high dielectric constant. Rather, the Patent Office simply states that the dielectric material disclosed by Shinichi "obviously" includes a high dielectric constant. Such a blatantly bald and unfounded assertion of inherency is contrary to the tenets of

established patent laws and is a thoroughly improper determination of inherency. It is respectfully submitted that there is no suggestion, disclosure or teaching in Shinichi to support the Patent Office's assertion of inherency. Rather, it is respectfully submitted that the Patent Office is basing its determination of inherency on mere "probabilities or possibilities." The Patent Office has proffered no evidence that makes it clear that "the missing descriptive matter is *necessarily present* in the thing described in the reference."

Applicants respectfully traverse the assertion of inherency and request that the Patent Office cite a document in support of this determination so that the Applicants have a full and fair opportunity to respond to the combination of documents.

In addition, according to M.P.E.P. § 2142, "[t]o reach a proper determination under 35 U.S.C. 103, . . . impermissible hindsight must be avoided and the legal conclusion [of obviousness] must be reached on the basis of the facts gleaned from the prior art." Furthermore, according to M.P.E.P. § 2143.01, "[t]he mere fact that references can be . . . modified does not render the resultant combination obvious unless the prior art also suggests the desirability of [such modification]." [citing *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990)] It is respectfully submitted that there is no disclosure or suggestion in Shinichi that the dielectric material can be "any" dielectric material, in particular a dielectric material with a high dielectric constant. It is respectfully submitted that the Patent Office's determination of inherency and its assertion that the dielectric material comprises a high dielectric constant is completely without support in Shinichi or otherwise. Therefore, it is respectfully submitted that the Patent Office's attempt to modify Shinichi for its rejection based on obviousness is clearly and unequivocally founded upon "knowledge gleaned only

from Applicant's disclosure." [*see* M.P.E.P. § 2145] Consequently, it is respectfully submitted that the rejection entails hindsight and is, therefore, improper.

Independent claims 97, 106, 115, 122 and 129 recite features similar to those discussed above with respect to independent claim 88, and are, therefore, patentably distinguishable over the Shinichi for at least those reasons stated above with regard to independent claim 88.

Dependent claims 89-90, 92-96, 98-99, 101-105, 107-108, 110-114, 116-117, 119-121, 123-124, 126-128, 130-131 and 133-135 variously depend from independent claims 88, 97, 106, 115, 122 and 129, and are, therefore, patentably distinguishable over Shinichi for at least those reasons stated above with regard to independent claims 88, 97, 106, 115, 122 and 129.

For at least the foregoing reasons, it is respectfully submitted that Shinichi does not render the subject matter of claims 88-90, 92-99, 101-108, 110-117, 119-124, 126-131 and 133-135 unpatentable. Accordingly, reconsideration and withdrawal of these grounds of rejection are respectfully requested.

All of the rejections raised in the Office Action having been addressed, it is respectfully submitted that the present application is in condition for allowance and a notice to that effect is earnestly solicited. Should the Examiner have any questions regarding this response or the application in general, the Examiner is urged to contact the Applicants' attorney, Andrew J. Bateman, by telephone at (202) 625-3547. All correspondence should continue to be directed to the address given below.

Respectfully submitted,

By: Andrew J. Bateman

Andrew J. Bateman
Attorney for Applicants
Registration No. 45,573

IP Docket
Katten Muchin Zavis Rosenman
1025 Thomas Jefferson St., NW
East Lobby, Suite 700
Washington, DC 20007-5201
Facsimile No.: (202) 298-7570

Customer No.: 28285